**Claim Amendments:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A method comprising:
when in a first mode of operation, utilizing a first output coupled to a memory to provide a first data lane enable for facilitating access of a portion of a first memory storage location of the memory associated with a first memory address; and
when in a second mode of operation, utilizing the first output to provide an address bit of a second memory address for facilitating designation of a second memory storage location of the memory.

2. (Original) The method of claim 1 wherein:
the first data lane enable facilitates accessing a byte of data associated with the first memory address when in the first mode of operation; and
the second memory address accesses a byte wide memory.

3. (Original) The method of claim 1 wherein:
the first data lane enable facilitates accessing a byte of data associated with the first memory address when in the first mode of operation; and
the second memory address accesses a word wide memory.

4. (Previously Presented) The method of claim 3 wherein the number of bits associated with the word wide memory is greater than eight.

5. (Previously Presented) The method of claim 1 wherein:
the first output is the first output of a first device; and
the first and second modes of operation utilize the first output to access a second device external the first device.

6. (Previously Presented) The method of claim 5 further comprising:

when in a third mode of operation, utilizing the first output to provide information about a memory access internal to the device that includes the first output.

7. (Previously Presented) A method comprising:

when in a first mode of operation, utilizing a first output to provide a first data lane enable for facilitating access of a portion of a first memory storage location associated with a first memory address; and

when in a second mode of operation, utilizing the first output to provide an address bit of a second memory address for facilitating designation of a second memory storage location, wherein the address bit is an additional address bit used to extend an address range when a memory having a width less than a word width is being accessed.

8. (Previously Presented) The method of claim 1, further comprising:

determining a mode of operation to be one of the first mode of operation and the second mode of operation.

9. (Previously Presented) The method of claim 8, wherein:

determining the mode of operation is based upon a register value associated with a specific chip select.

10. (Original) The method of claim 1 further comprising:

when in the first mode of operation, utilizing a second output to provide an address bit of the first memory address for facilitating designation of the first memory storage location; and

when in the second mode of operation, utilizing the second output to provide a second data lane enable for facilitating access of a portion of the second memory storage location associated with the second memory address.

11. (Previously Presented) A method of providing data to a set of pins of a device, the set of pins coupled to a memory, the method comprising:

during a first mode of operation, multiplexing a first set of data onto the set of pins to allow the set of pins to provide data representing two least significant bits of a first address, a most significant bit of the first address, and a lane enable;

during a second mode of operation, multiplexing a second set of data onto the set of pins to allow the set of pins to provide data representing one least significant bit of a second address, a most significant bit of the second address, and two lane enables; and

during a third mode of operation, multiplexing a third set of data onto the set of pins to allow the set of pins to provide four lane enables.

12. (Original) The method of claim 11, wherein the first, second and third sets of data facilitate an external memory access, wherein the external memory access is external relative to the device.

13. (Previously Presented) The method of claim 12, further comprising:

during a fourth mode of operation multiplexing a fourth set of data onto the set of pins to allow the set of pins to provide information relating to an internal memory access.

14. (Previously Presented) The method of claim 11 further comprising:

determining the mode of operation is based upon a chip select indicator.

15. (Previously Presented) An apparatus comprising:

a set of address nodes coupled to a memory to provide address data for address bit locations A(n) through A(2), where A(n) represents a most significant bit for at least a first mode of operation;

a first output node coupled to the memory to provide one of an address data for address bit location A(1) and a data lane enable signal based upon a mode of operation;

a second output node coupled to the memory to provide one of an address data for address bit location A(0) and a data lane enable signal based upon the mode of operation; and

a third output node coupled to the memory to provide one of an address data for address bit location A(n+1) and a data lane enable signal based upon the mode of operation.

16. (Previously Presented) An apparatus comprising:

a first register having an output to indicate one of a first mode of operation and a second mode of operation;

an address control portion having an input coupled to the output of the first register, and an output to indicate a value of an address bit when in the first mode of operation;

a first data lane enable control portion having an input coupled to the output of the first register, and an output to indicate a first data lane enable value when in the second mode of operation; and

an output pin coupled to the output of the address control portion and the output of the first data lane enable control portion, and further coupled to a memory.

17. (Previously Presented) The apparatus of claim 16 further comprising a multiplexor having a control input coupled to the output of the first register, a first data input coupled to the address control pin, a second data input coupled to the first data lane enable, and an output coupled to the output pin.

18. (Original) The apparatus of claim 16, wherein the first register is associated with one of a plurality of chip selects.

19. (Previously Presented) A system comprising:

a processing module coupled to a set of outputs; and

memory operably coupled to the processing module, wherein the memory stores operational instructions that cause the processing module to:

utilize a first output coupled to the memory to provide a first data lane enable to facilitate accessing of a portion of a first memory storage location of the memory associated with a first memory address when in a first mode of operation; and

utilize the first output to provide an address bit of a second memory address to facilitate designation of a second memory storage location of the memory when in a second mode of operation.

20. (Original) The system of claim 19 further comprising:

operational instructions that cause the processing module to:

when in a third mode of operation, utilize the first output to provide information about a memory access internal to the device.

21. (Previously Presented)A method of operating a microcomputer comprising:

when the microcomputer is in a first mode of operation, utilizing a first output of a microcomputer to provide a first data lane enable to a memory for facilitating access of a portion of a first memory storage location of the memory associated with a first memory address; and

when the microcomputer is in a second mode of operation, utilizing the first output of the microcomputer to provide an address bit of a second memory address to the memory for facilitating designation of a second memory storage location of the memory.